Electronic Version
Stylesheet Version v1.1.1

MODULAR DLL ARCHITECTURE FOR GENERATING MULTIPLE TIMINGS

Abstract

A modular Digital Locked Loop (DLL) architecture capable of generating a plurality of multiple phase clock signals, having particular applicability to synchronization of embedded DRAM systems with on chip timing. The architecture comprises a single core frequency locking circuit that includes a delay element with control logic and locking circuitry capable of locking the DLL system clock frequency to an external reference clock, and a plurality of secondary phase locking circuits capable of synchronizing a plurality of internal clock signals to any phase of the external reference clock.